

Figure 1 - DT/IT processes up to IT CMP

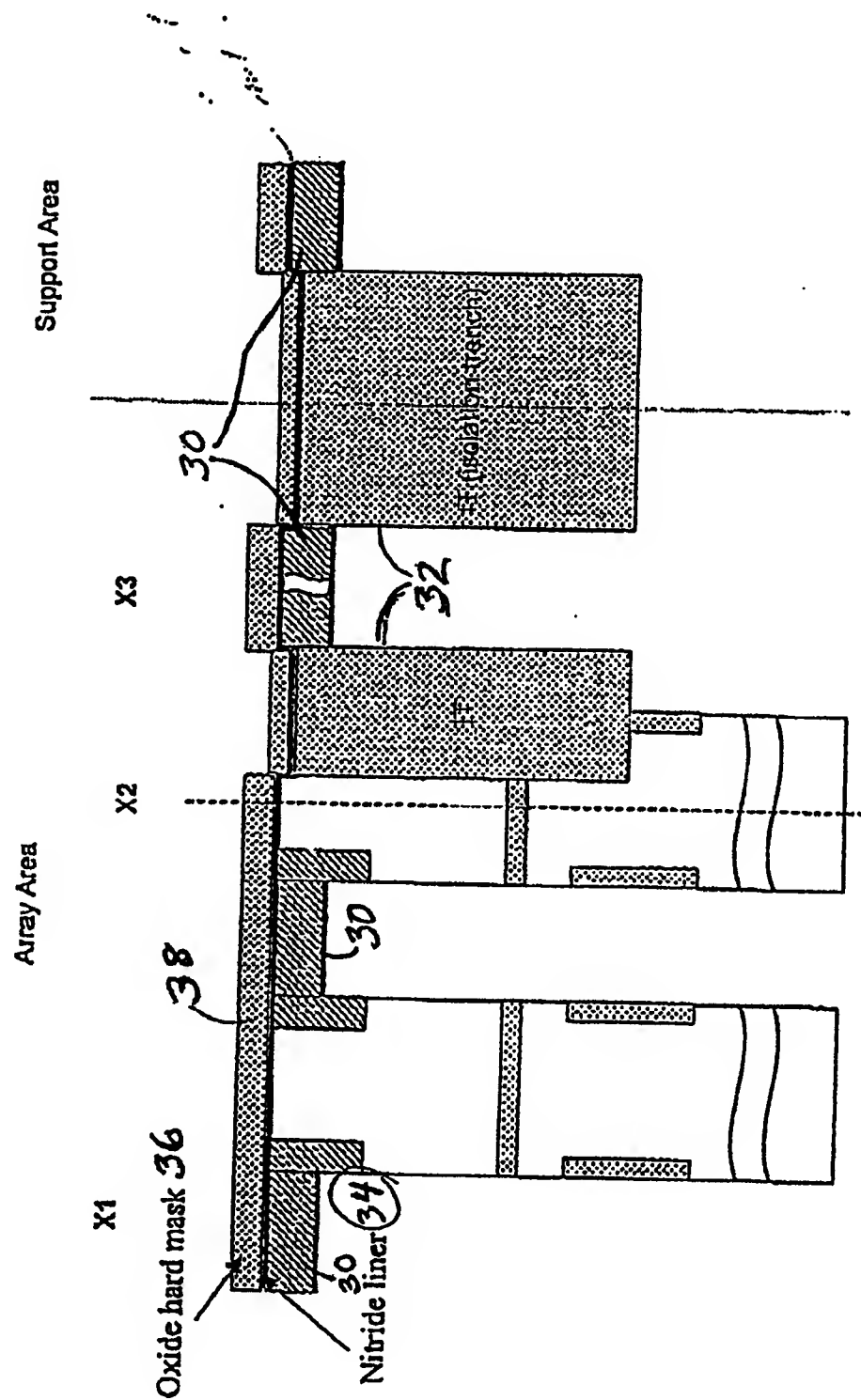


Figure 3 -- Deglaze/Nitride liner dep (optional)/Oxide mask dep

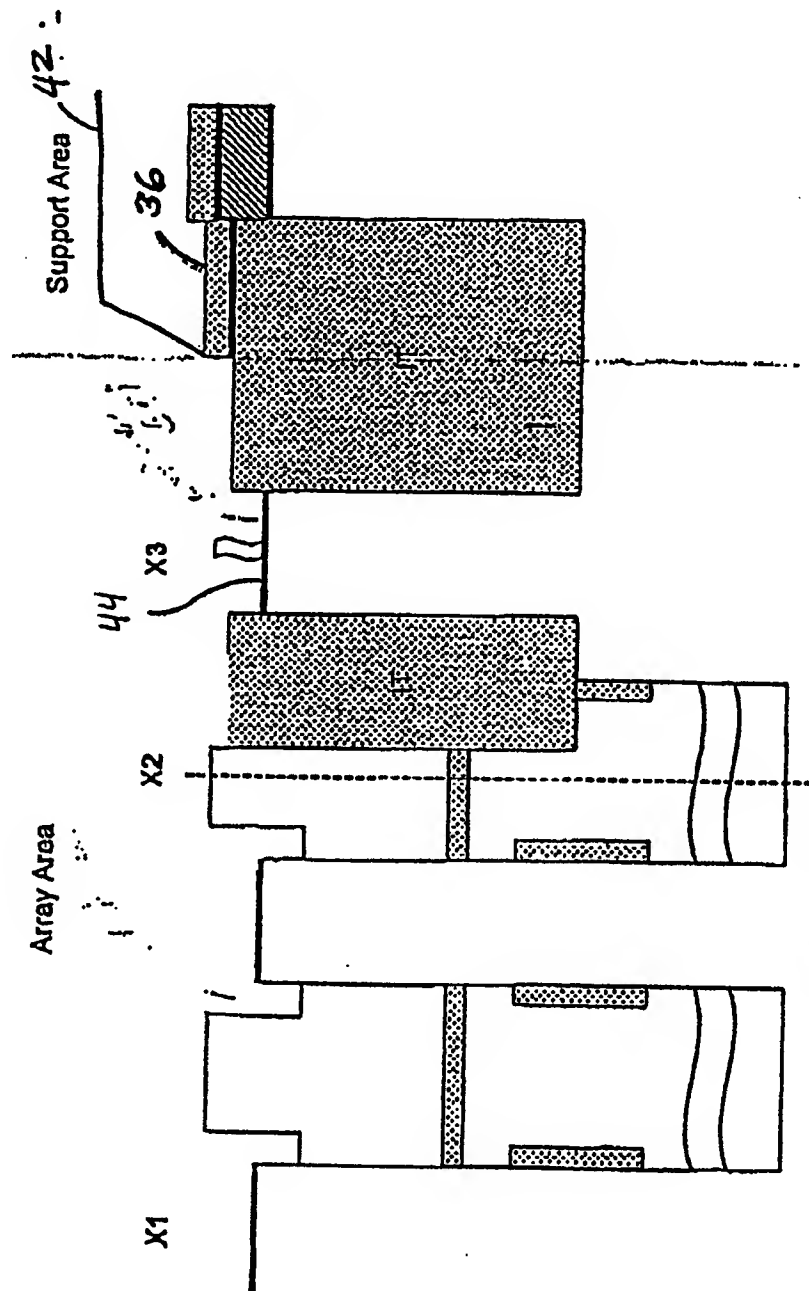


Figure 4 - EA litho (block mask)/oxide etch in array/resist strip/Nitride liner, nitride spacer & pad nitride strip in array/Pad oxide strip/regrow pad oxide

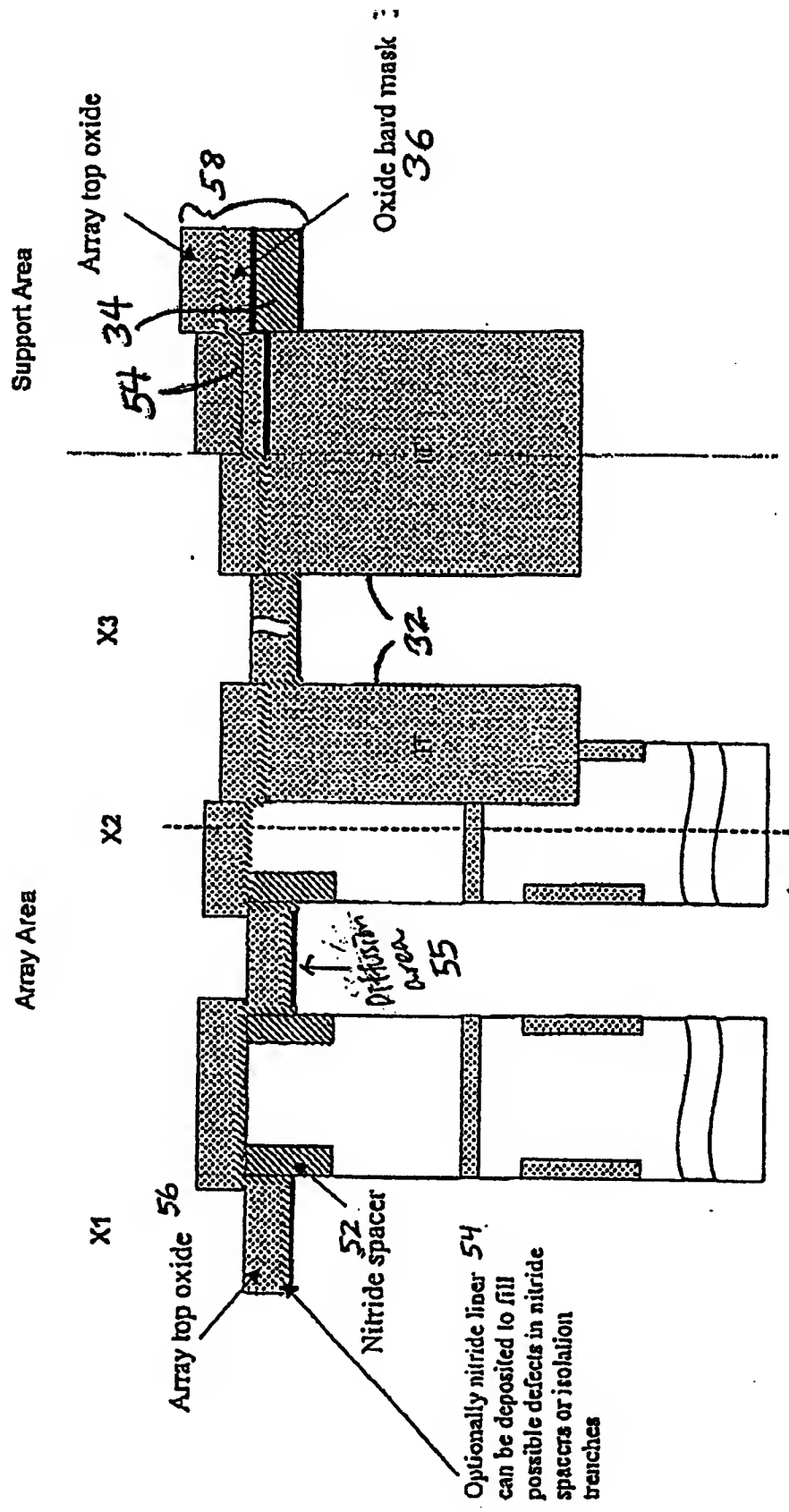


Figure 5 - Nitride spacer dep & etch/Array implants/
Nitride liner dep to fill possible defects in nitride spacer or IT (optional)/Array top oxide dep

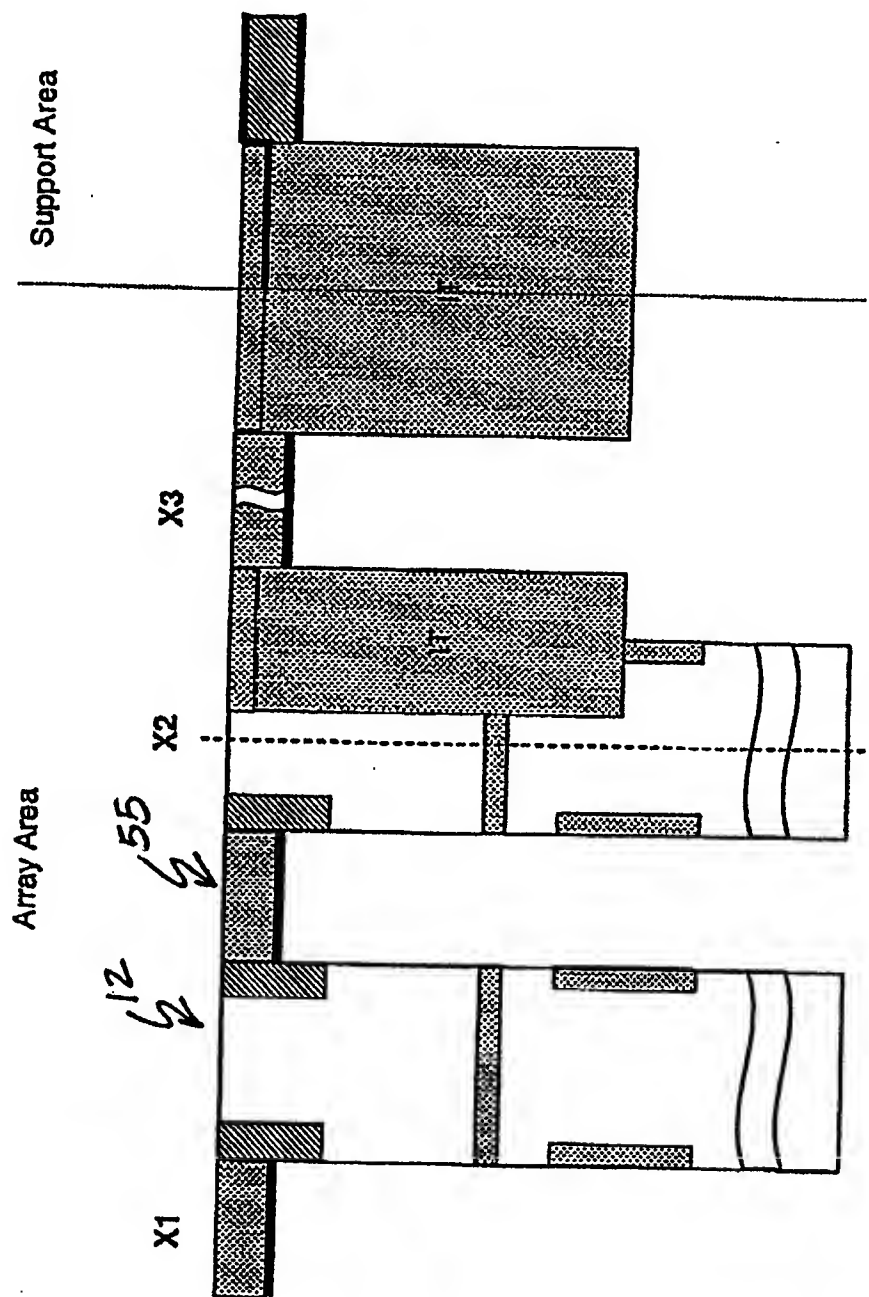


Figure 6 - ATO CMP (or ARC planarization)

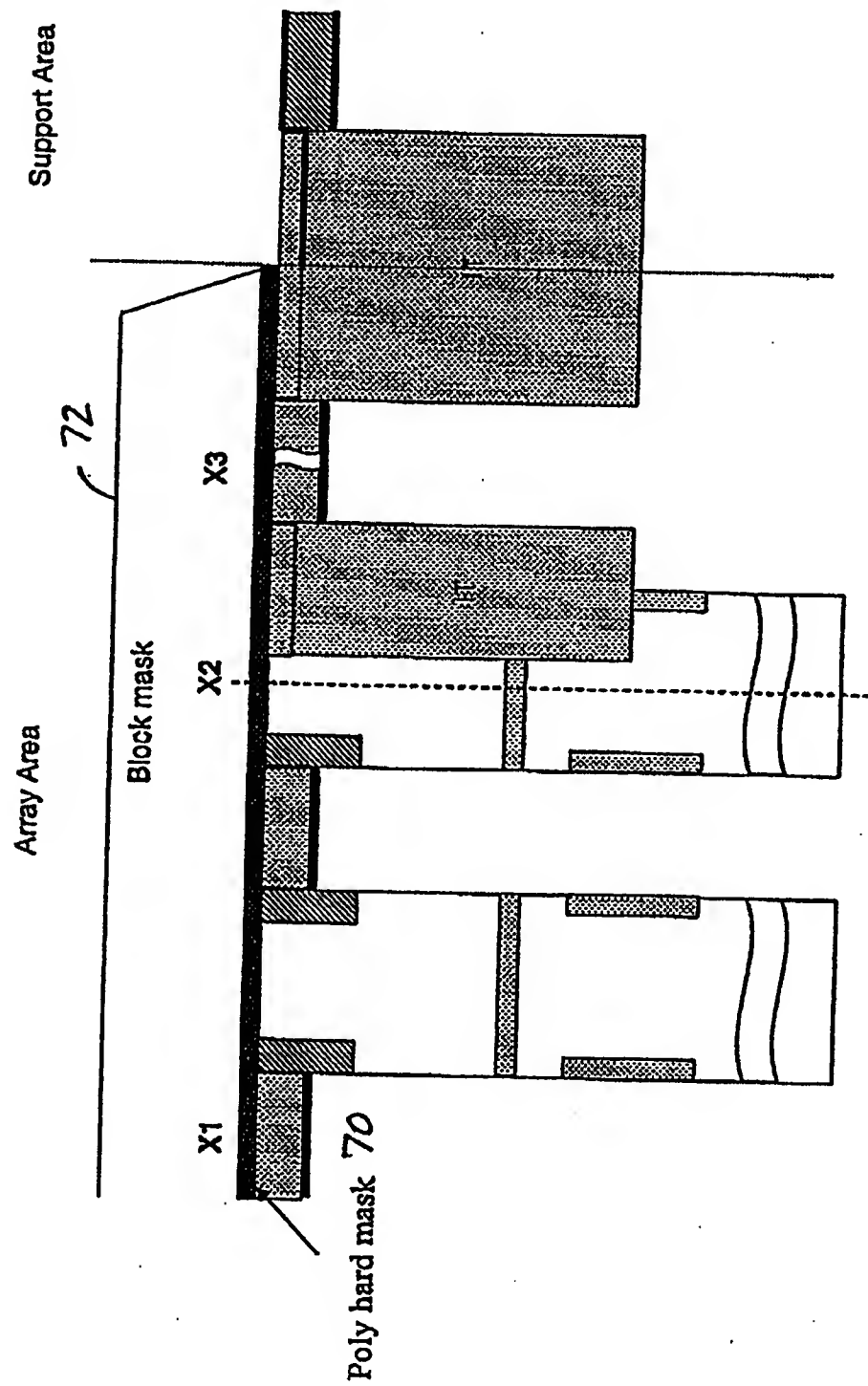


Figure 7 - Poly dep/ES litho/poly etch in support/resist strip

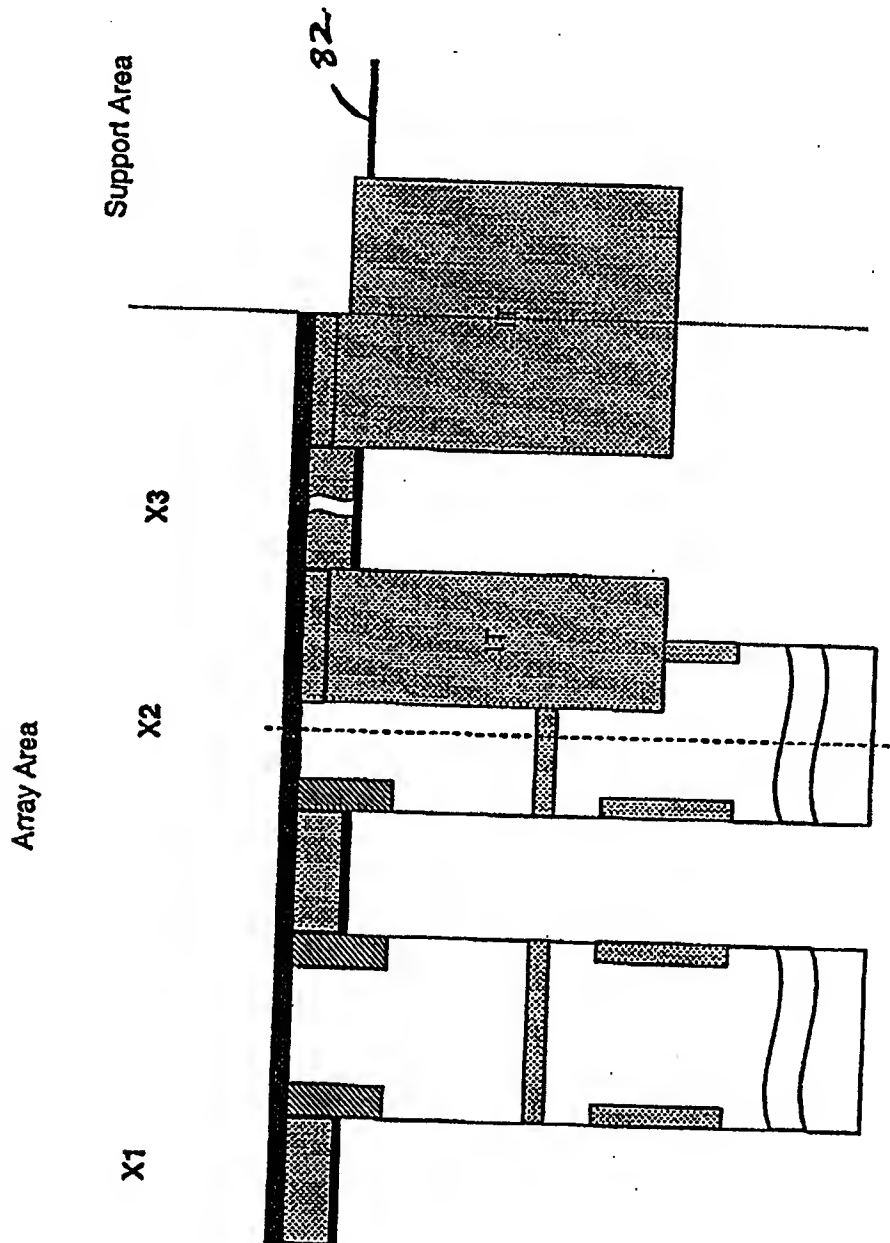


Figure 8 - Etch oxide, nitride liner & IT oxide to a desired height/Strip pad nitride in support/Pad oxide strip & sac ox growth in support/Support implants

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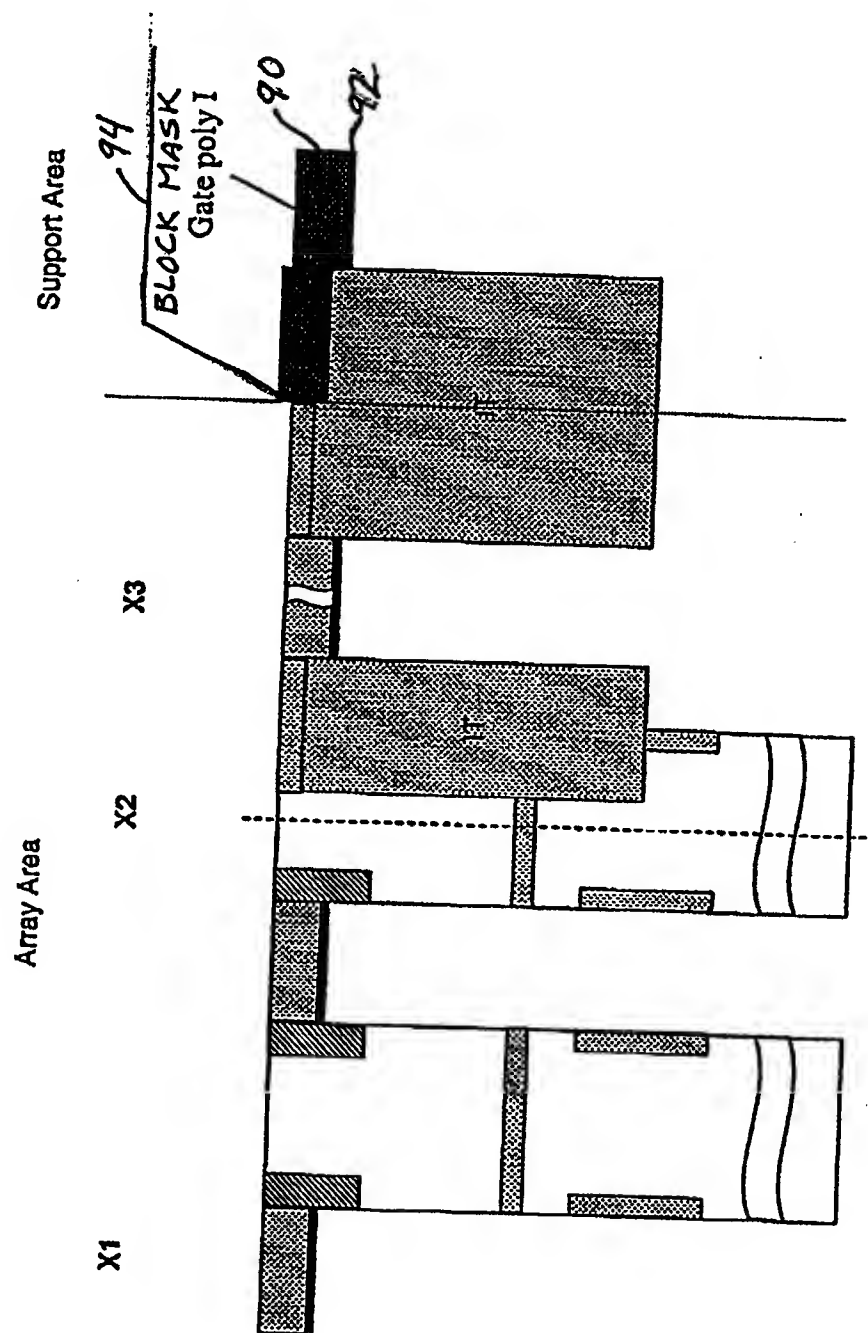


Figure 9 - Gate ox/WL's/BL's formation and BEOL processes

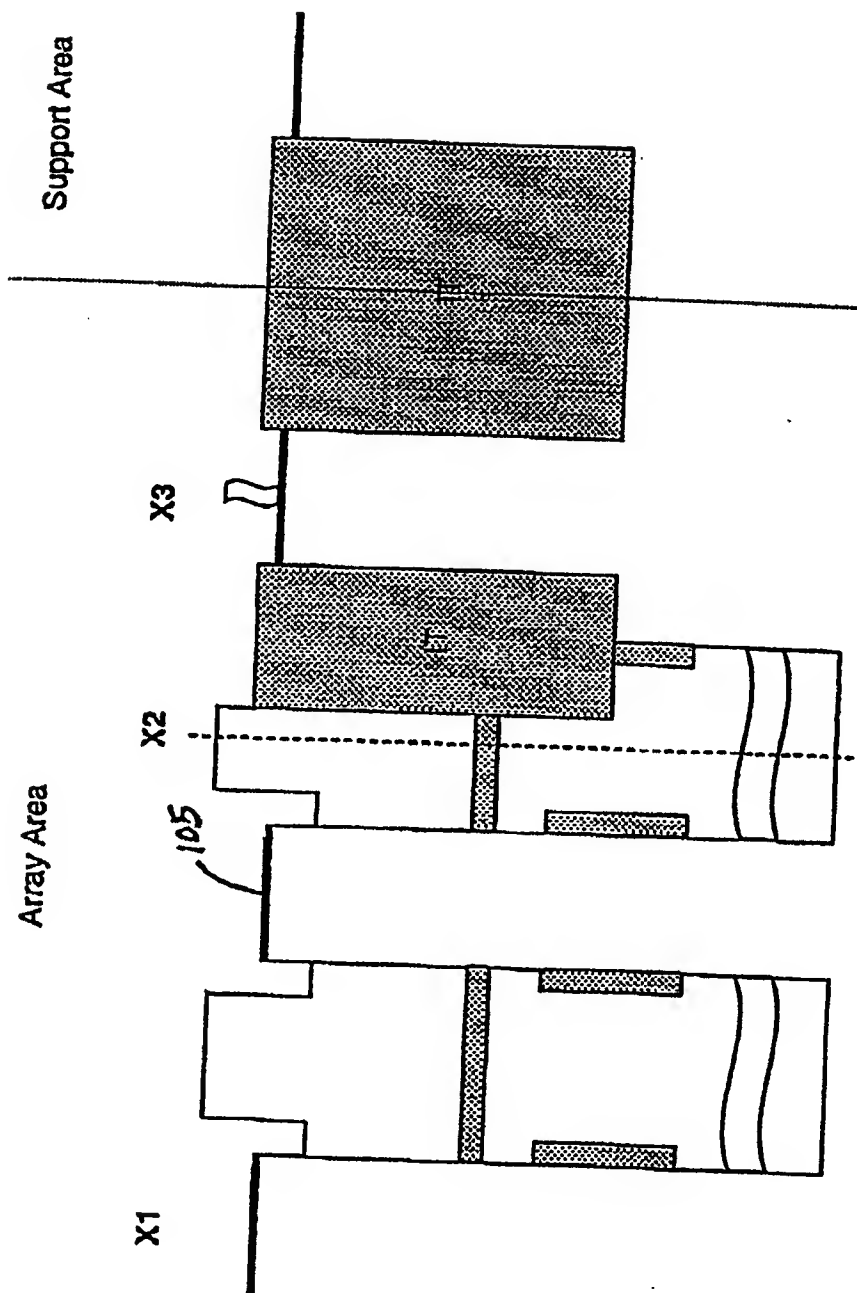


Figure 10 - Deglaze/Pad nitride strip/Pad oxide strip/pad reox

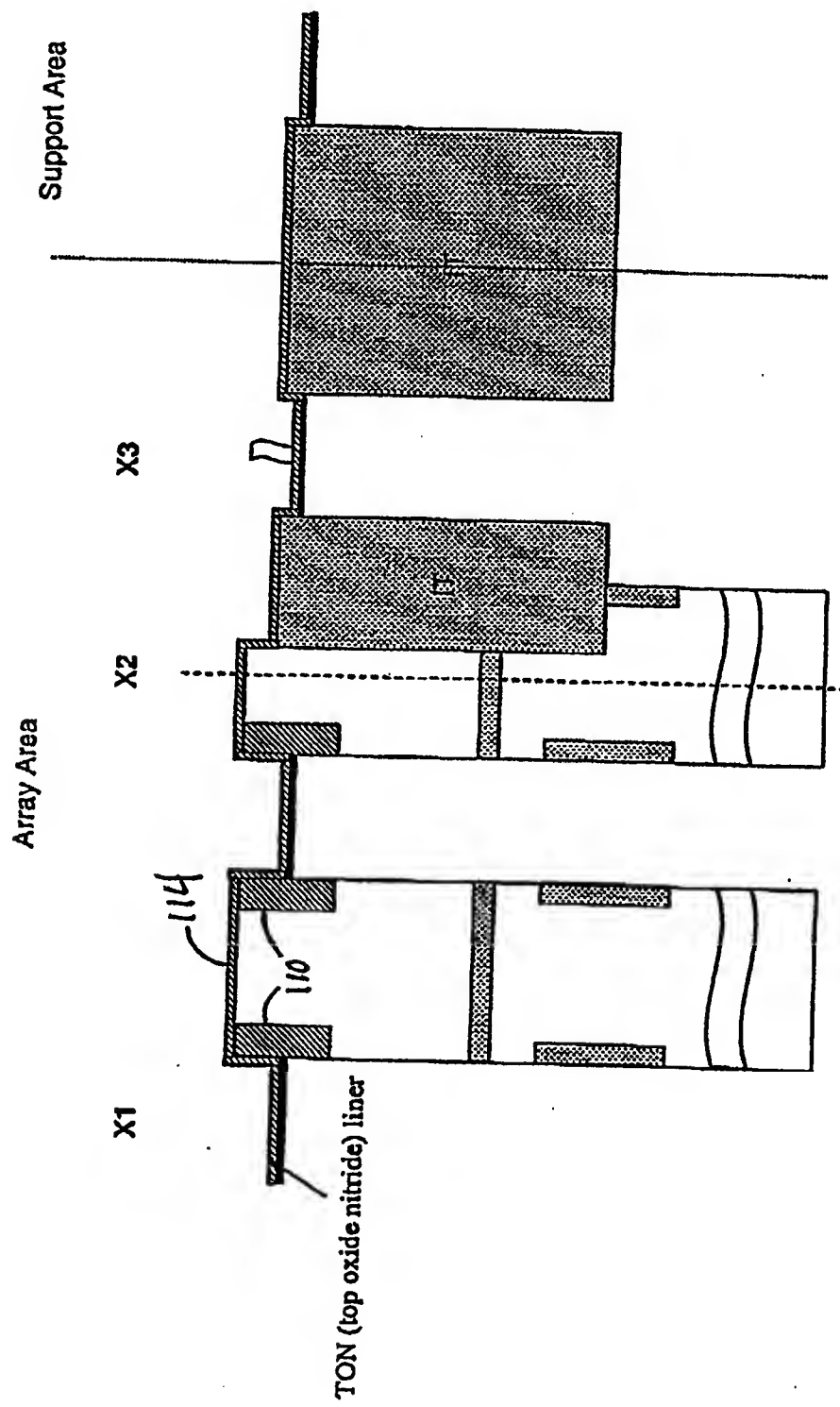


Figure 11—Nitride spacer formation/Array implants/TON liner

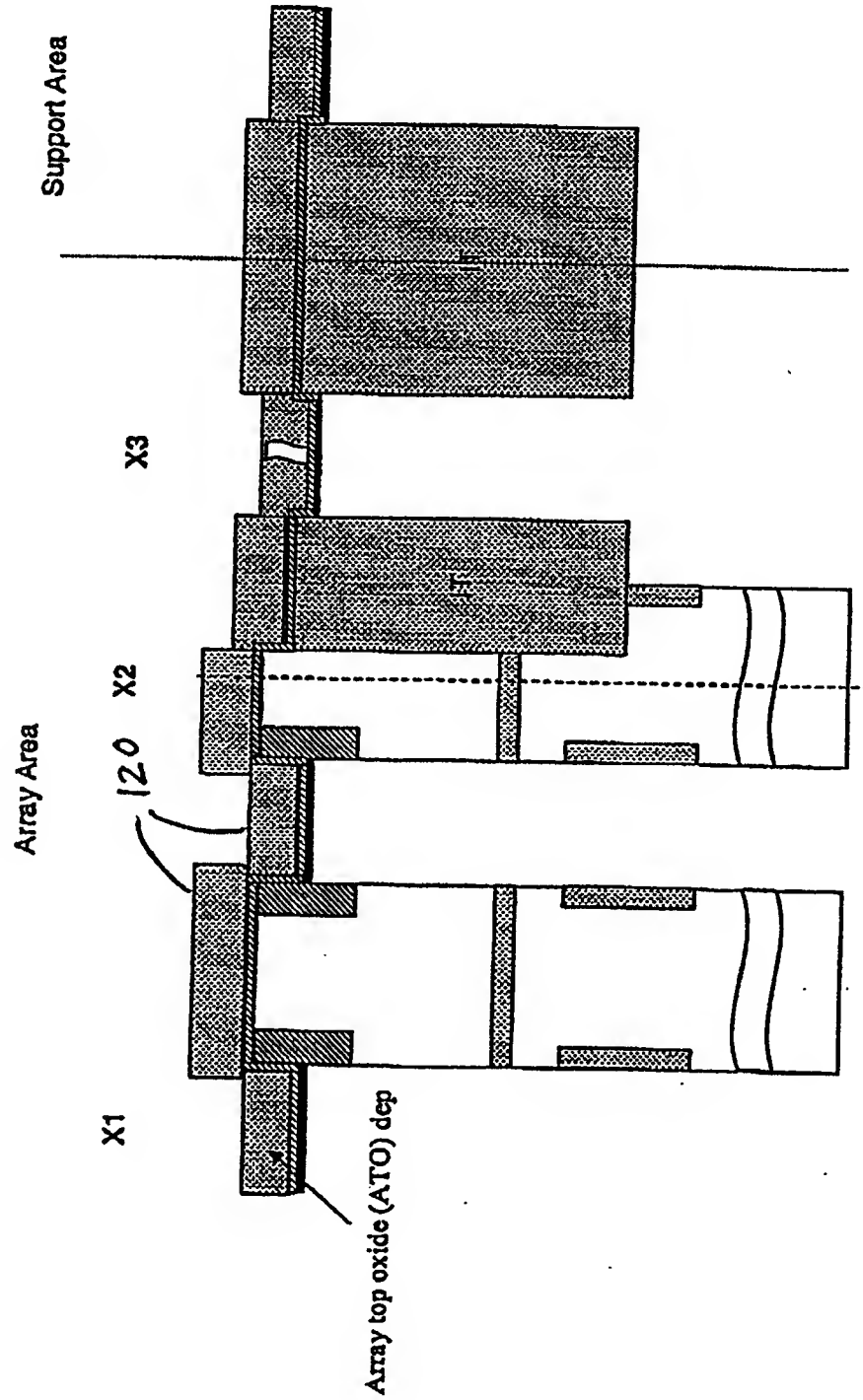


Figure 12-Array top oxide dep

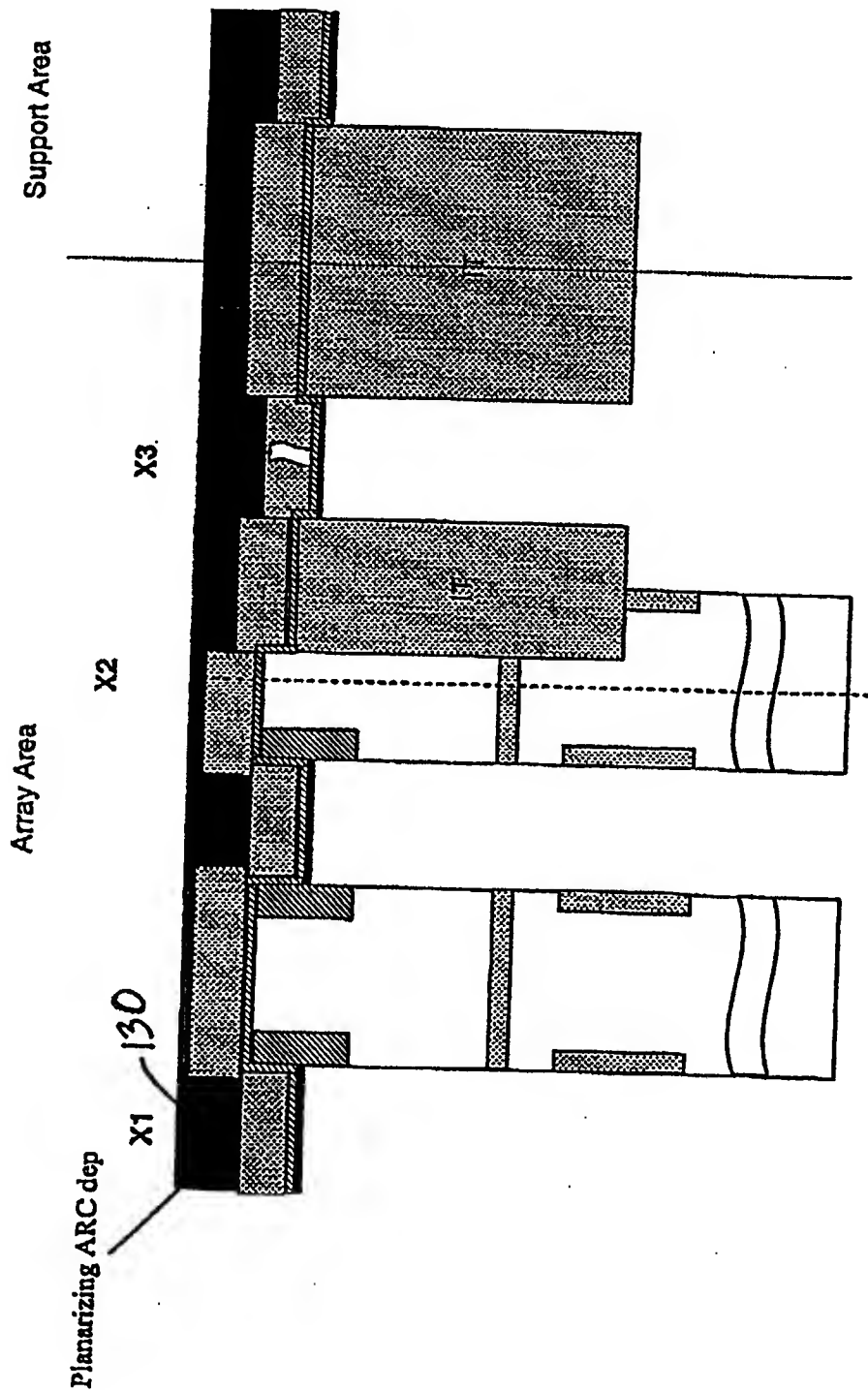


Figure 13a Planarizing ARC dep

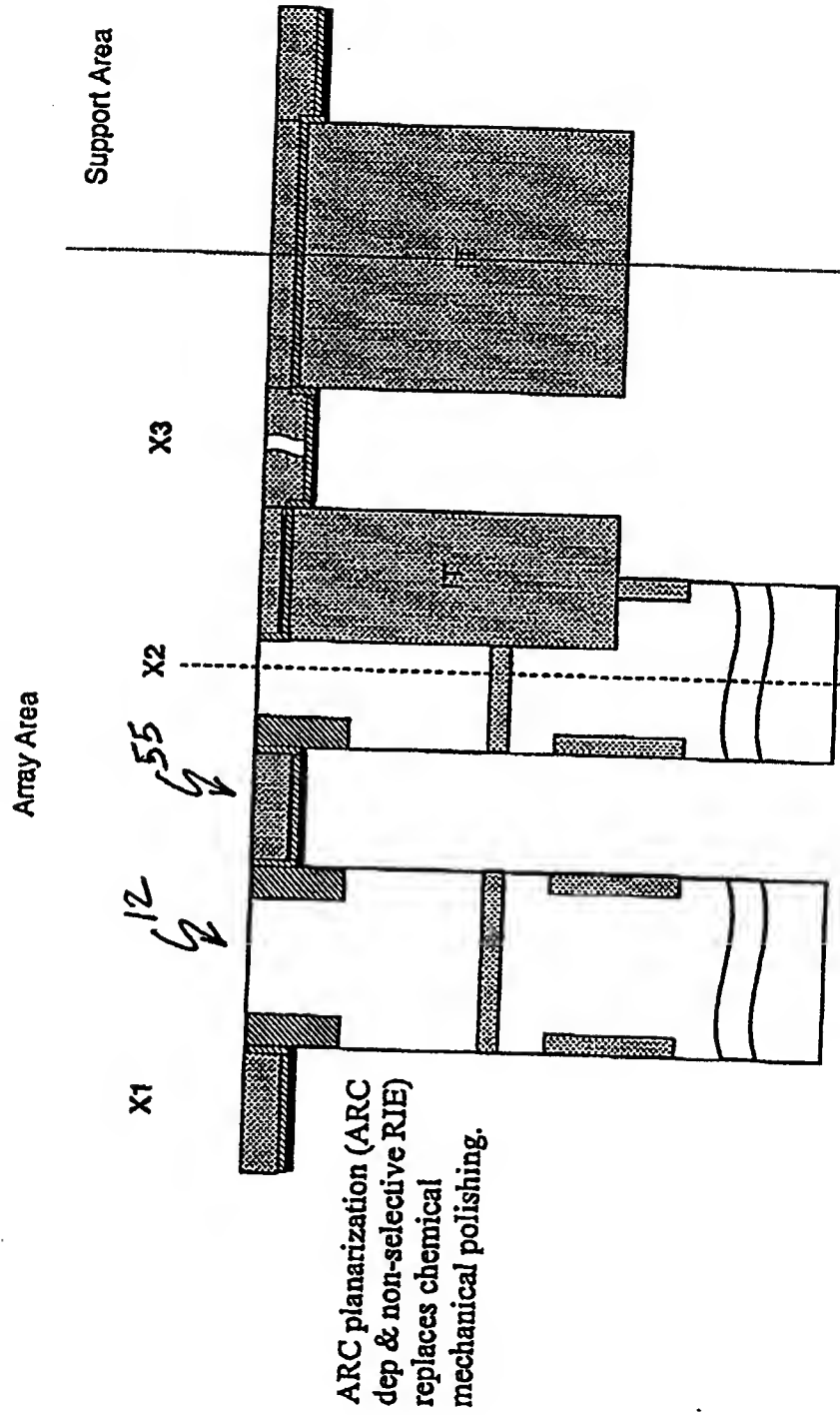


Figure 14: Non-selective RIE to remove oxide on DT stud

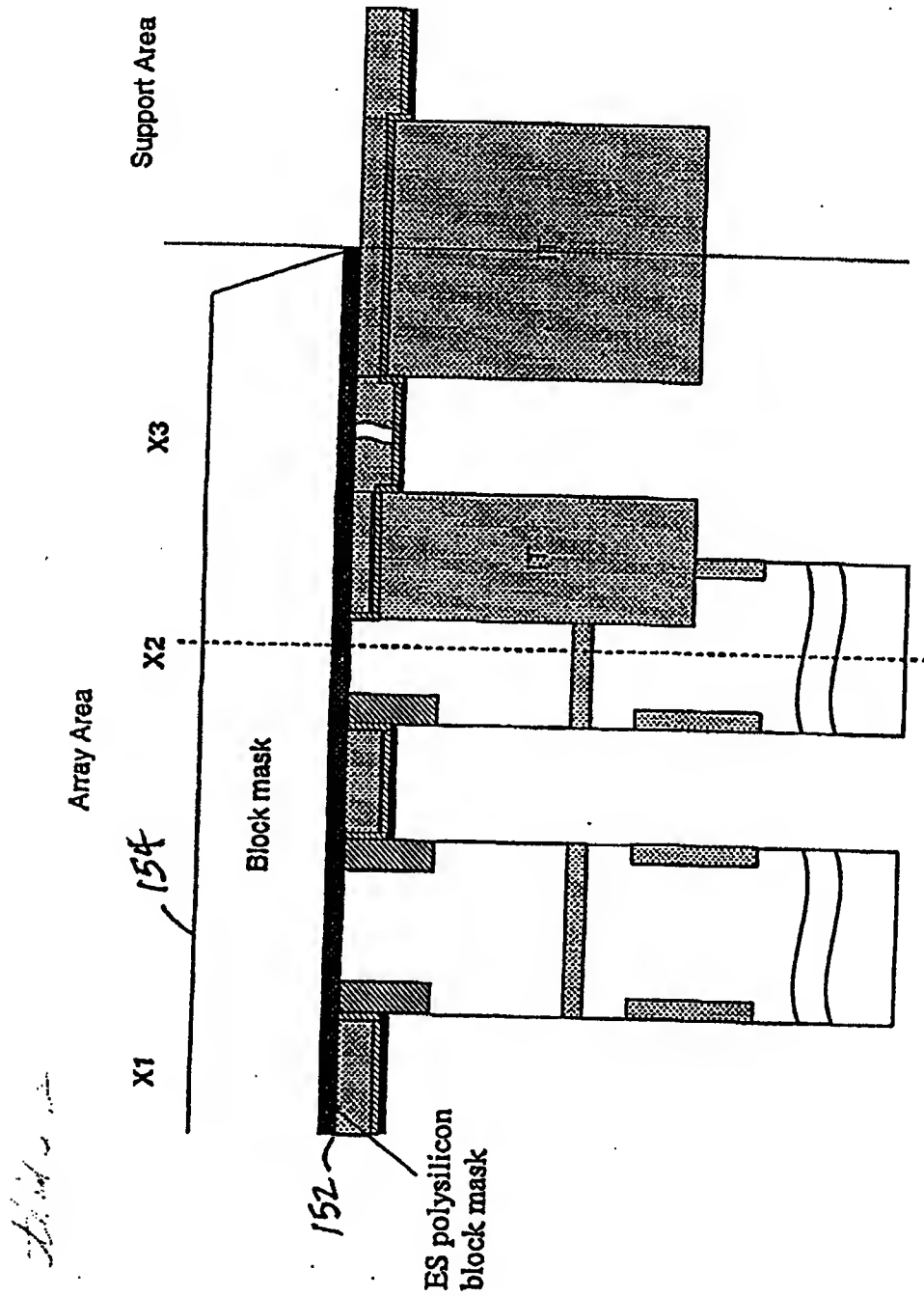


Figure 11b- ES poly dep/block mask/poly etch in support/resist strip/
Continue with gate conductor/WL/BL/BEOL formation.

Schematics of TOL with ARC planarization & height equalization between array and support

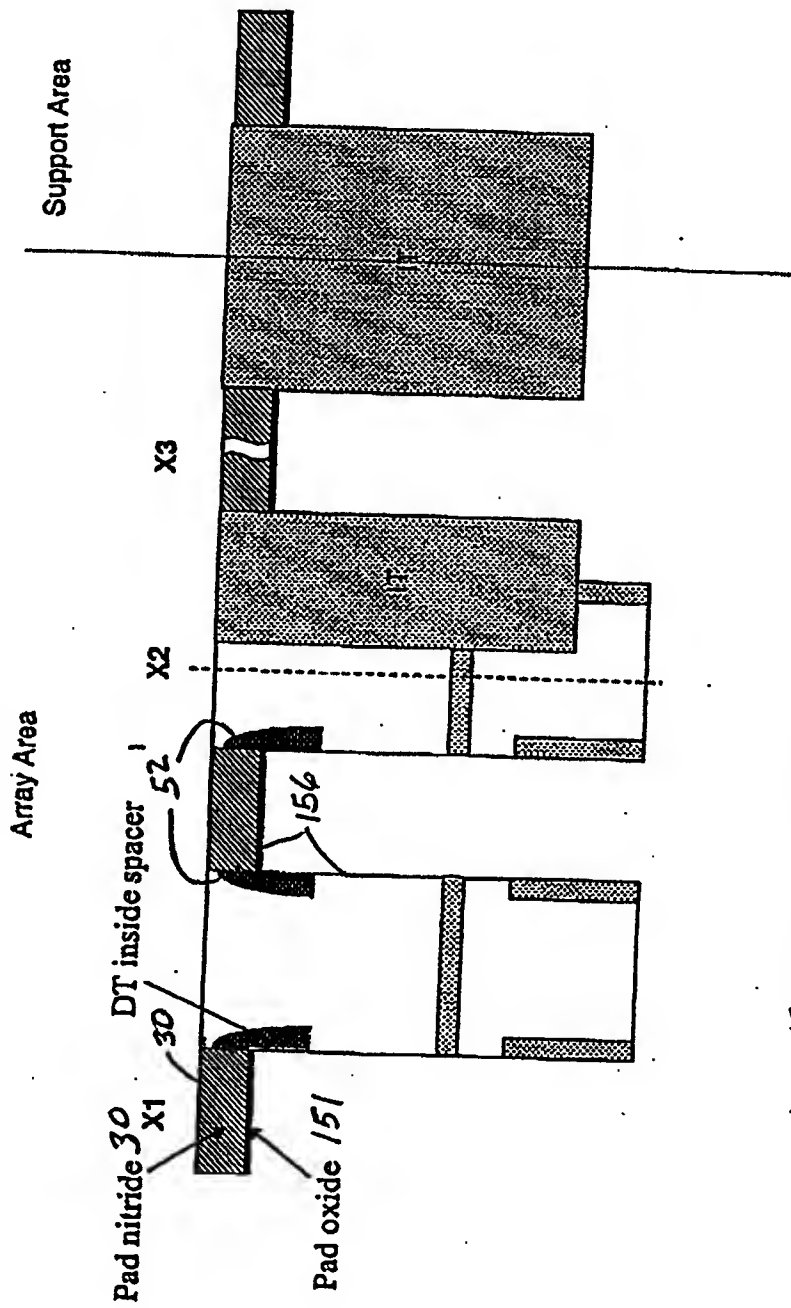


FIGURE 15A - DT and IT processes up to IT CMP

Schematics of TOL with ARC planarization & height equalization between array and support

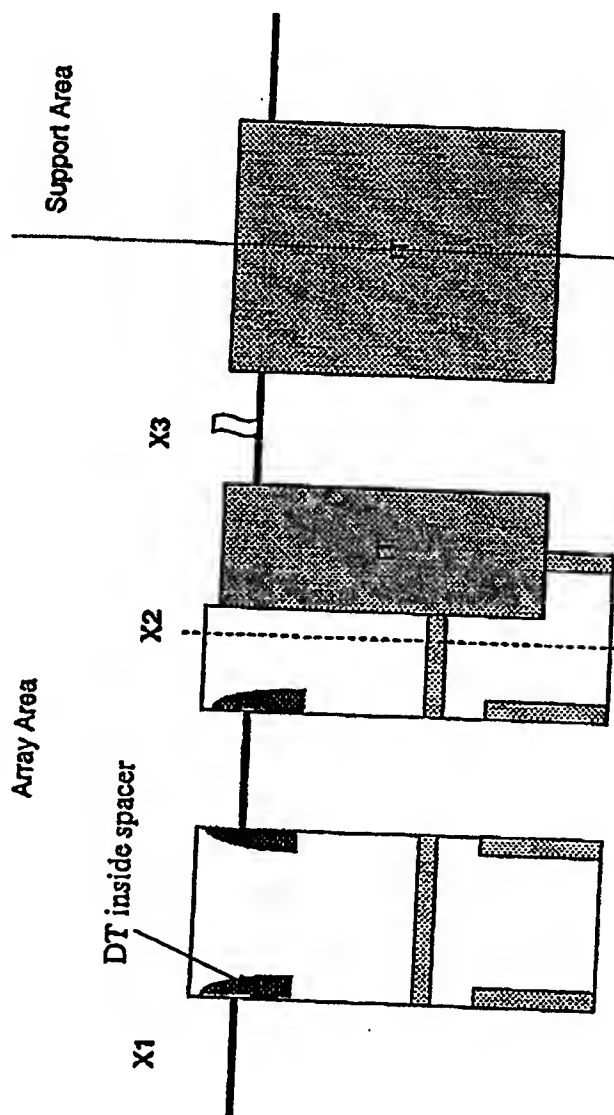
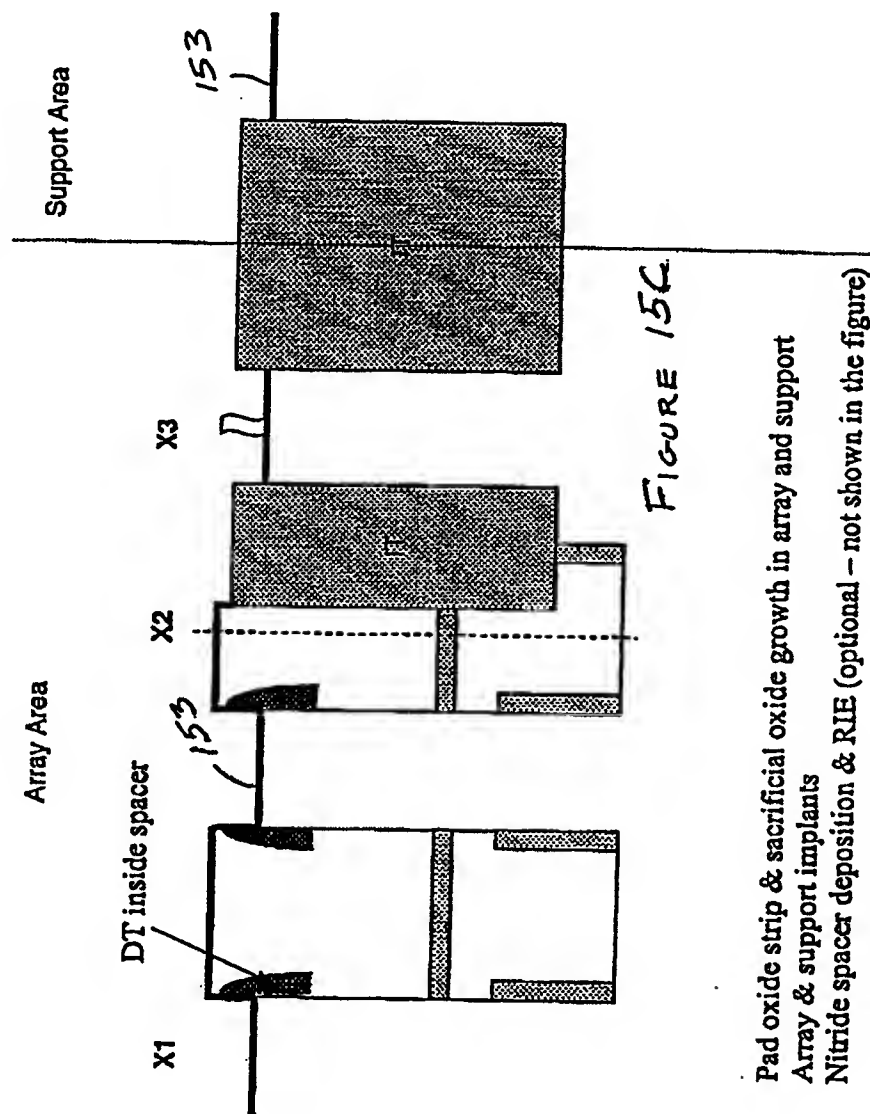


FIGURE 15B

Deglaze (etching of IT oxide in array and support)
 Pad nitride strip in array and support (This process is DT inside spacer conservation process and DT inside spacer is not stripped during pad nitride strip. The DT inside spacer is protected by vertical gate oxide.)

Schematics of TOL with ARC planarization & height equalization between array and support



Schematics of TOL with ARC planarization & height equalization between array and support

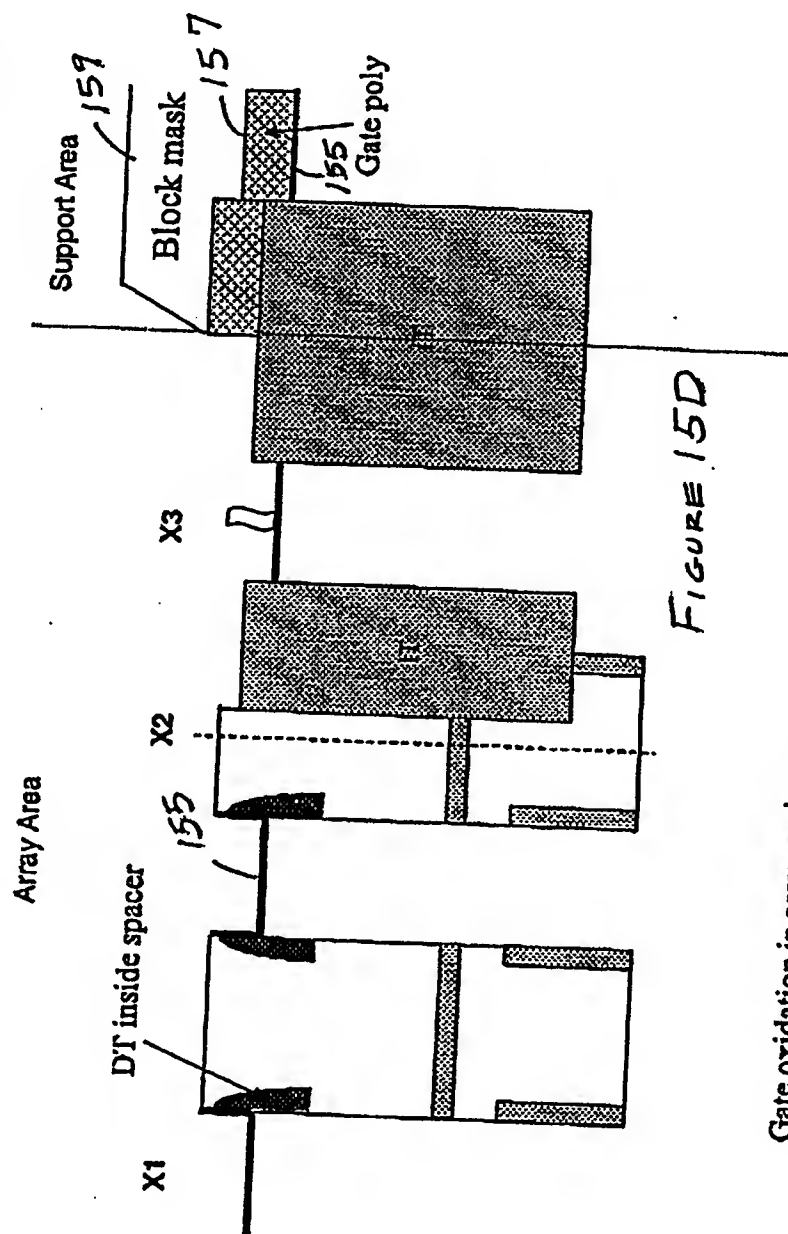


FIGURE 15D

Gate oxidation in array and support
 Gate poly deposition in array and support
 Block mask to protect support/etch gate poly in array/resist strip

Schematics of TOL with ARC planarization & height equalization between array and support

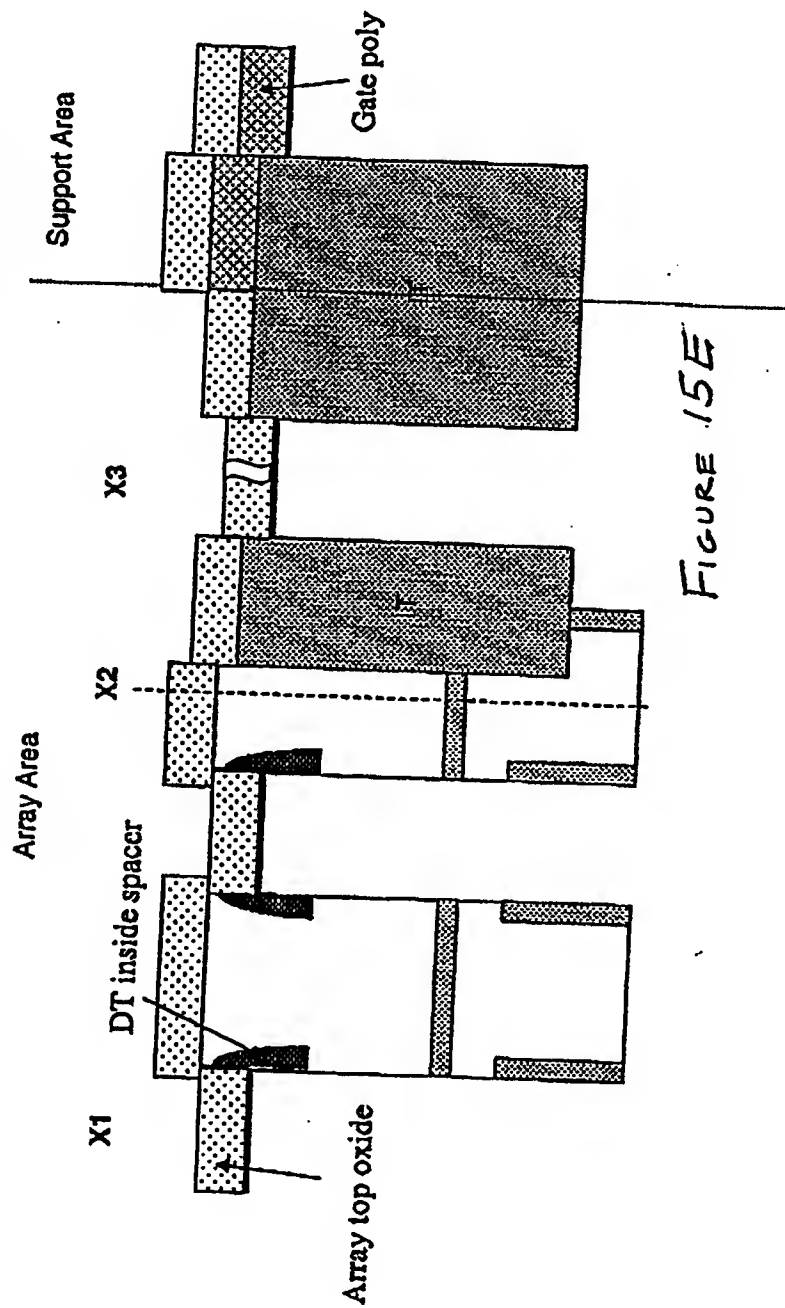


FIGURE 15E

Schematics of TOL with ARC planarization & height equalization between array and support

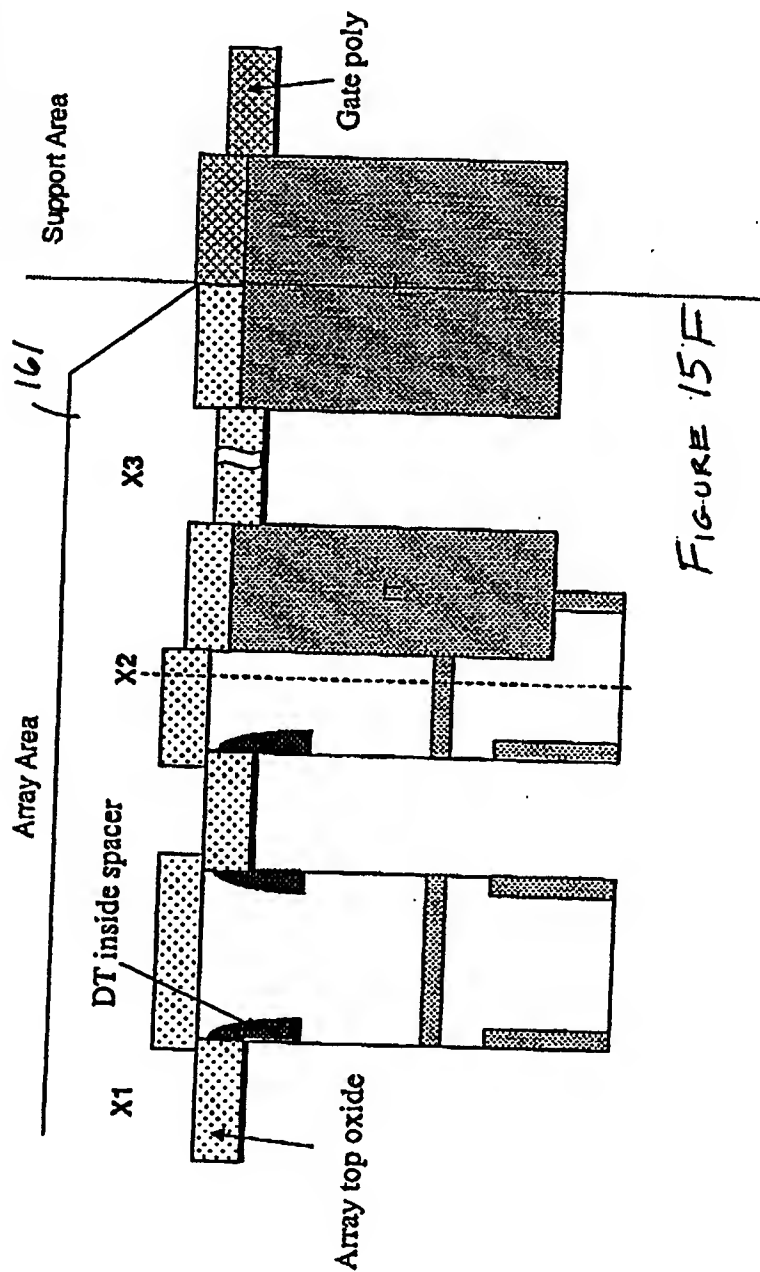


FIGURE 15F

Block mask to protect array/etch array top oxide in support to make the step height between array and support similar/resist strip (for Option II)

Schematics of TOL with ARC planarization & height equalization between array and support

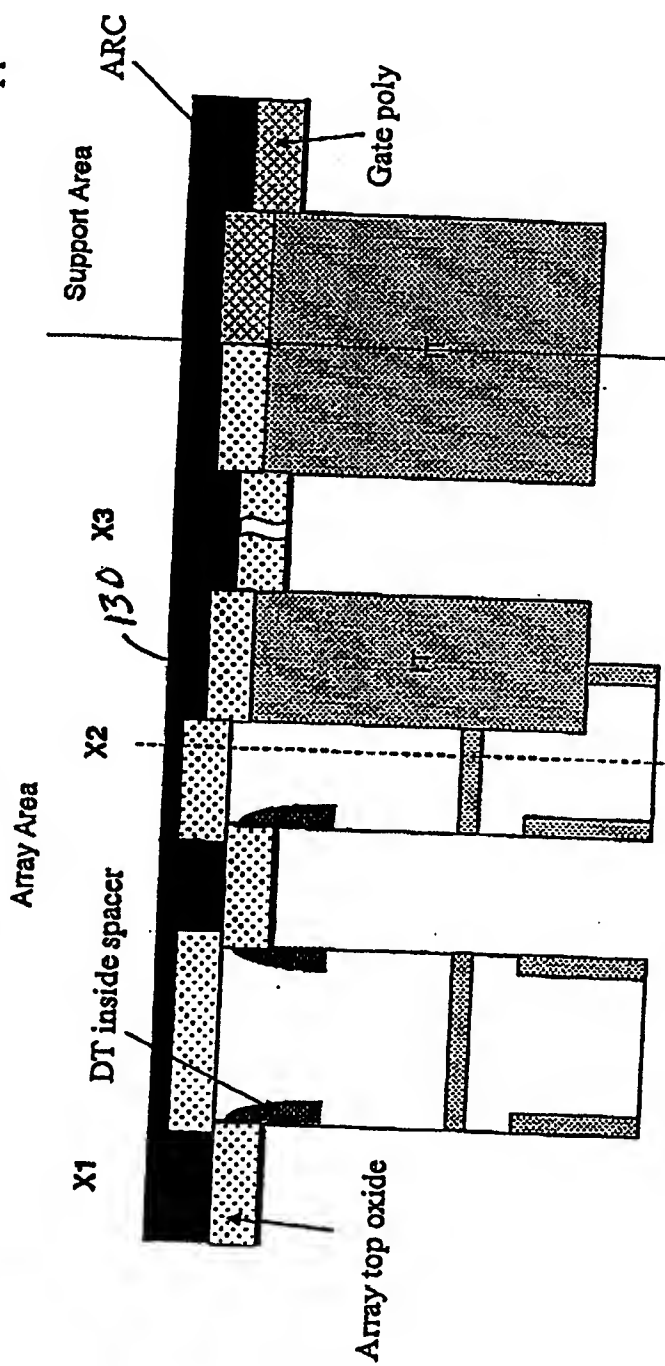


FIGURE 15G

ARC deposition

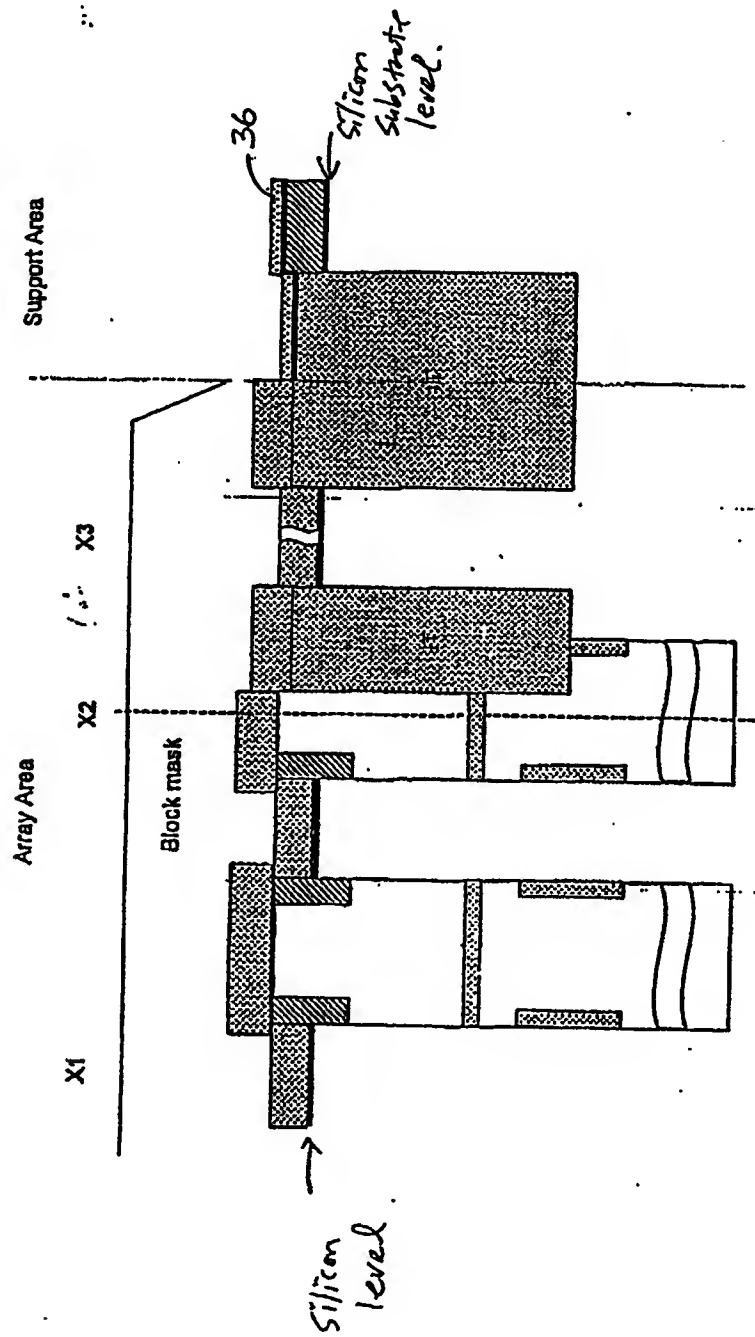


FIGURE 16 - Block mask/oxide etch in support (in order to make the average step height in support same as that in array)/strip

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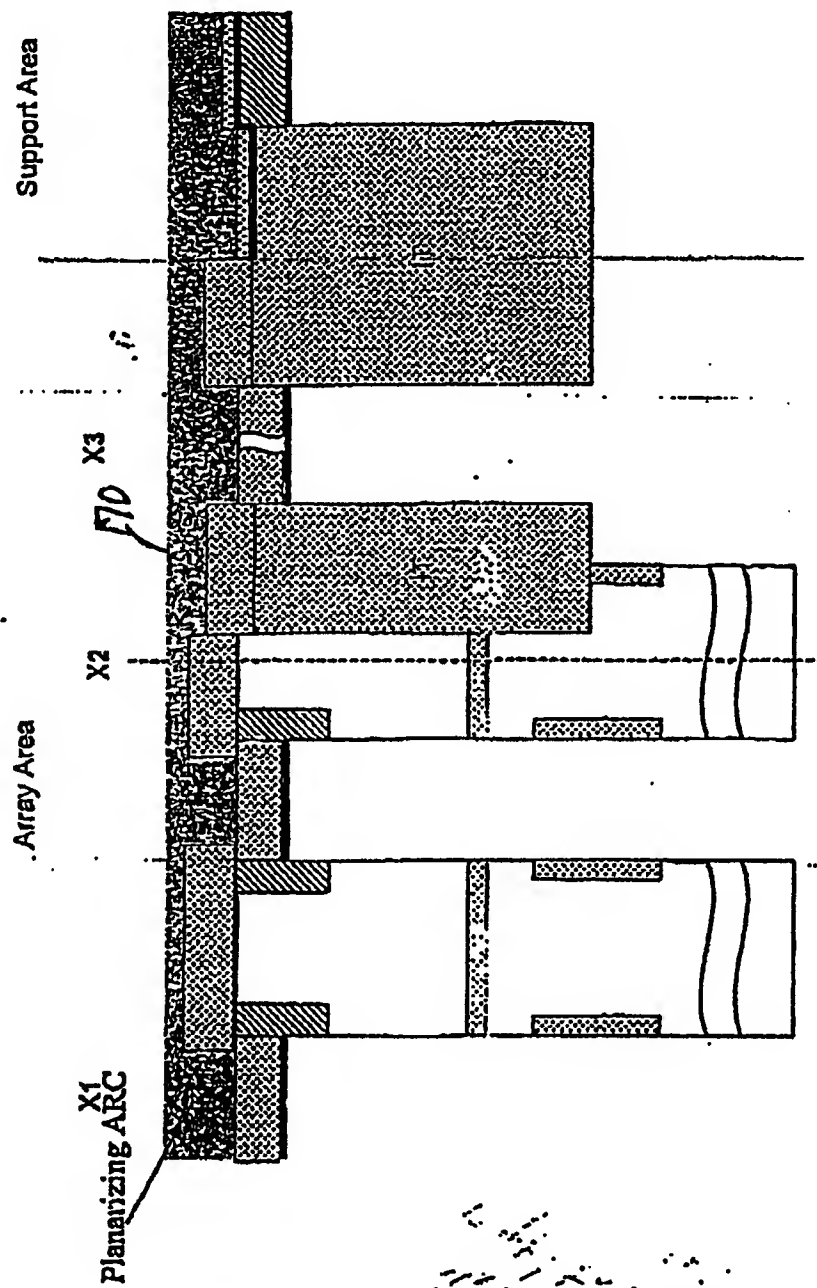
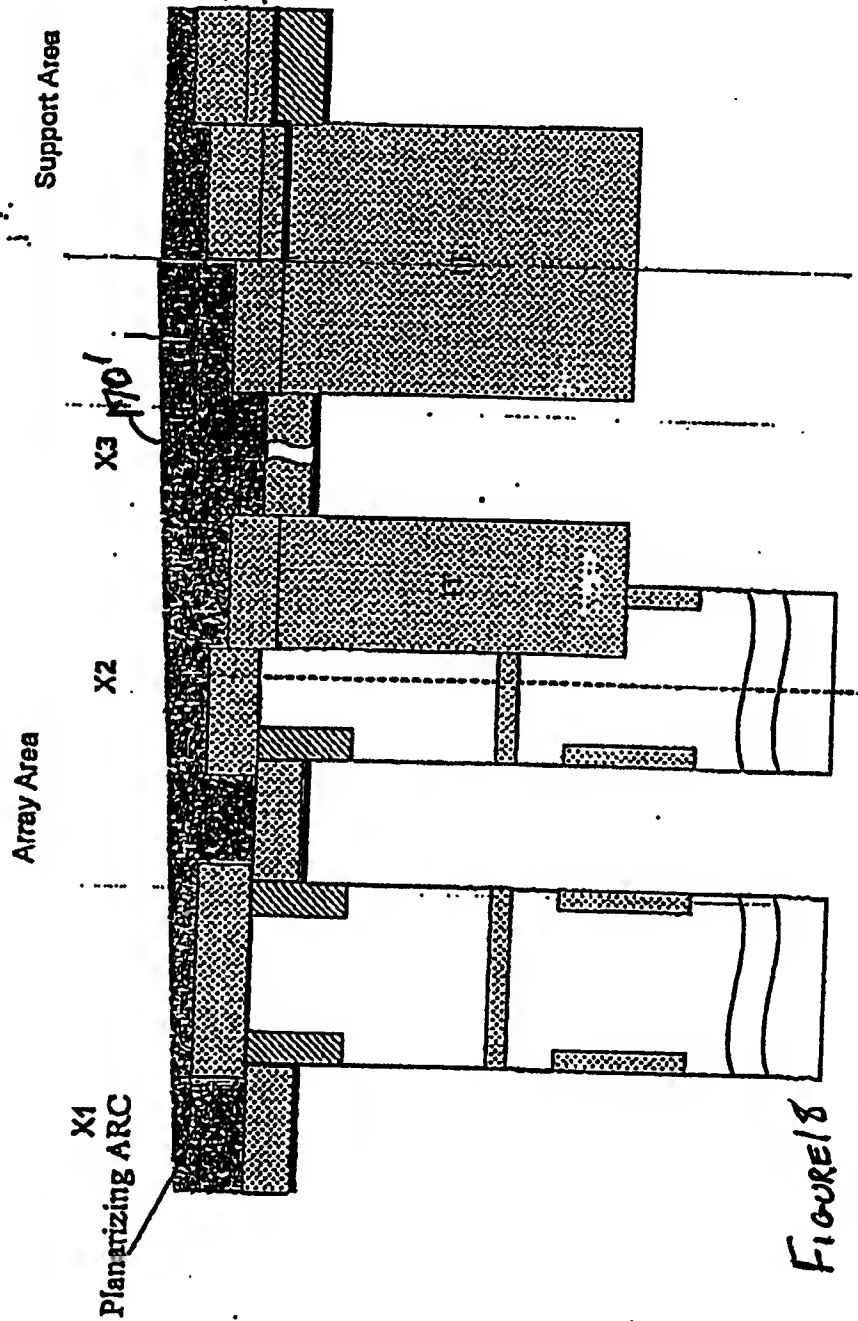


FIGURE 17 - planarizing ARC dep (profile with block mask/oxide etch in support/strip)



- Profile without block mask/oxide etch in support/resist strip (this is another disclosure - Improved TOE)

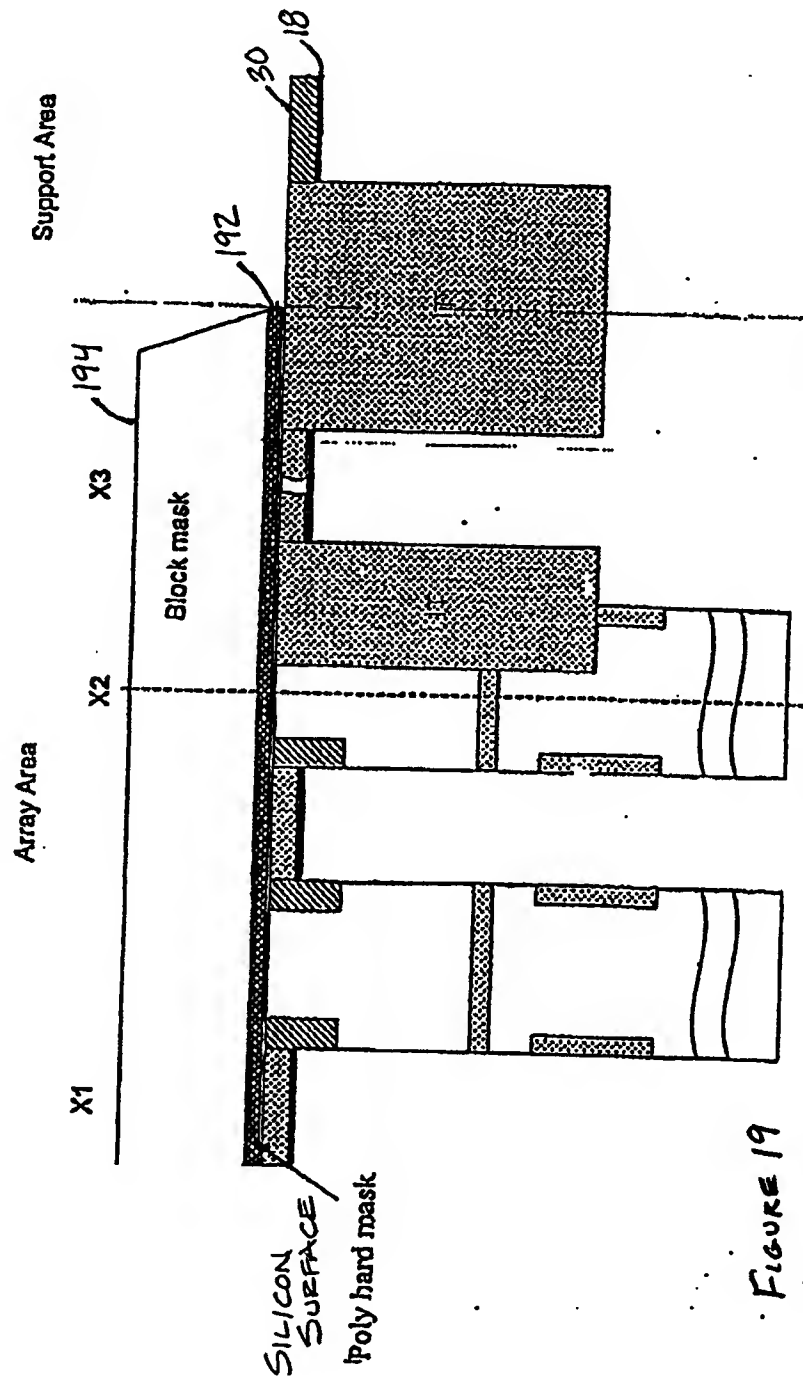


FIGURE 19

Non-selective ARC assisted RIE (this step replaces chemical mechanical polishing, can be controlled by end point)
 /ES poly dep/ES mask (block mask)/poly removal in support/slip

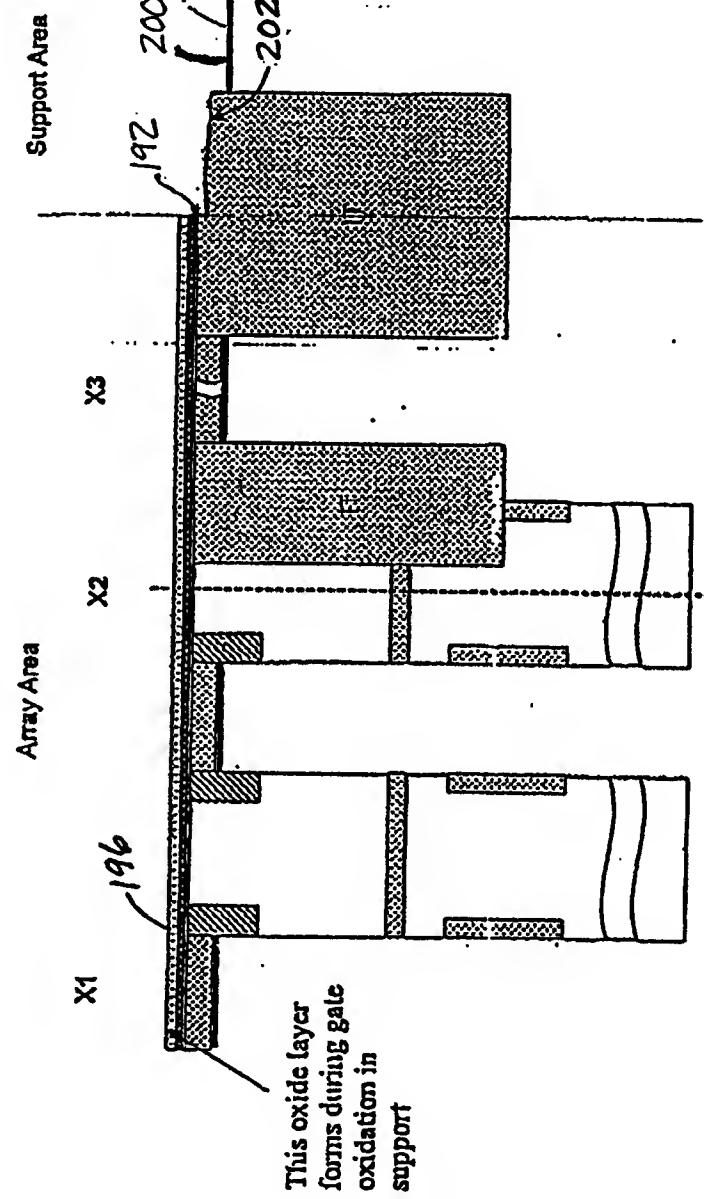


FIGURE 20. Etch oxide, nitride liner & IT oxide to a desired height/Strip pad nitride in support/Pad oxide strip & sac ox growth in support/Support implants

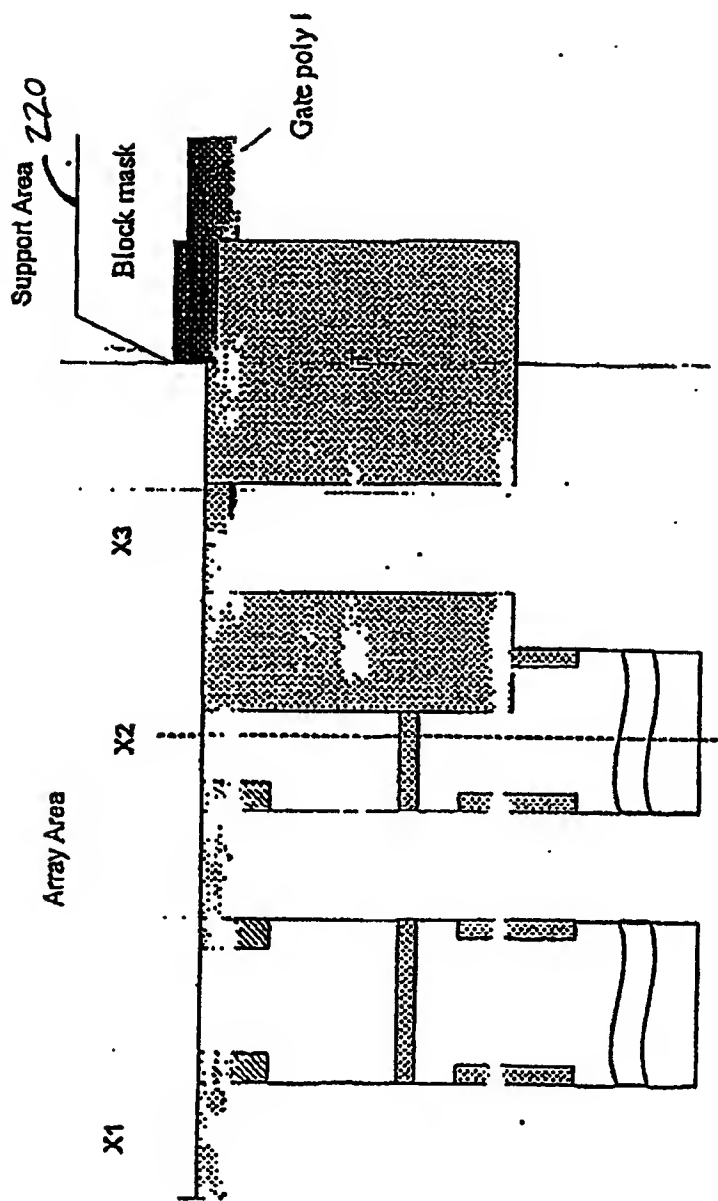


Figure 22 - Block mask/poly, oxide, poly etch in array/strip
Continue with WL's/BL's formation and BEOL processes